

CPC Technology Roadmap - Summary

STRATEGIES

2006

2007

2008

2009

2010

**Implement
State of the
Art
Interconnect
Fabrication
Processes**

**Roadmap
Summary**

Fine Circuit Trace Technologies:

.005" RCOG .004" SOA

.004" RCOG .002" SOA

.003" RCOG .002" SOA

Small Plated Hole Technologies (drilled hole diameter):

.012" RCOG .010" SOA

.010" RCOG .008" SOA

.010" RCOG .006" SOA

Microvia Technologies:

µvia dia. .006" RCOG .005" SOA

.004" RCOG .002" SOA

Pad dia. .012" RCOG .010" SOA

.010" RCOG .008" SOA

RF Material Bonding Technologies:

Arlon 6700, Speedboard

4450, Fusion, CLTE

Advanced HS/HF materials
High Perf Pb-free Materials

Buried Passive Technologies:

R's, C's +/- 15% RCOG R's, C's +/- 10% SOA

Layer Count:

16 Lyr RCOG 22 Lyr SOA

22 Lyr RCOG 30 Lyr SOA

22 Lyr RCOG 36 Lyr SOA

Registration Technologies (via / pad):

.016" / .036" RCOG
.012" / .022" SOA

.012" / .022" RCOG
.008" / .018" SOA

.008" / .018" RCOG
.008" / .016" SOA

RCOG: Revenue Center of Gravity (Toughest of 95% of the work)

SOA: State of the Art (Toughest 5% of the work)